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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/703,340	10/31/2000	Viktors Berstis	AUS9-2000-0733-US1	3090

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EXAMINER	
LINDINGER, MICHAEL L	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/703,340	BERSTIS ET AL.	
	Examiner	Art Unit	
	Michael L. Lindinger	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on 10 September 2002 is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to Claim 1-29 have been considered but are moot in view of the new ground(s) of rejection.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of copending Application No. 09/703,334, 09/703,335, and 09/703,344. Although the conflicting claims are not identical, they are not patentably distinct from each other because discloses a time cell, which experiences a transition of states after a programming

(charging) operation, detections means for detecting a value within a charge storage element, which is located within the time cell.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Drawings

1. The corrected or substitute drawings were received on September 10, 2002. These drawings are acceptable.

Specification

1. The corrected or substitute Specification was received on September 10, 2002. The Specification is acceptable.

2. The Applicant has explained the term "programming operation" sufficiently; therefore, the Examiner is withdrawing the objection to the Specification language in regards to this matter.

Claim Rejections - 35 USC § 112

1. The Applicant has amended the Claims to more clearly define the Claimed "reading means", therefore, the Examiner's rejection under 112 2nd paragraph is withdrawn.

Claim R jections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaki U.S. Patent No. 5,500,834 in view of Feddeler U.S. Patent No. 5,323,066. Regarding Claims 1-3, 24, 26-27, and 29, Sakaki teaches a horological device for measuring the time lapse after a turn off of a power source, wherein a capacitor is charged when power supplied to the system is turned on, wherein the capacitor is discharged when the power is disconnected, wherein the voltage of the capacitor is read and recorded by a processor when the power is turned, wherein the capacitor's value is also read and recorded when the power is turned off, wherein a corresponding time lapse is recorded, wherein inherently this teaches a time detection unit for processing a time request to generate a time response after reading the capacitor's value, thereby measuring the electrostatic charge of the capacitor, wherein the above mentioned elements combine to form claimed time cell (Col. 1, lines 10+; Col. 2, lines 25+; Col. 3, lines 1+; Col. 4, lines 5+; FIG. 1). Sakaki does not teach a horological device comprising a floating gate in a floating gate field effect transistor (FGFET), or explicit time determining means. Feddeler teaches a data acquisition means that

comprising a capacitor that is replaced with a floating gate in a floating gate field effect transistor (FGFET) (Col. 4, lines 12+; FIG. 5). It would have been obvious to a person skilled in the art at the time of the invention to not only adapt the Sakaki reference and include a floating gate in a floating gate field effect transistor (FGFET) in place of a capacitor in order to further insulate the charge element that is being charged and discharged, but to also to recognize that any capacitive timing device must inherently possesses the structure and means to read and interpret data as to whether or not a predetermined time period has elapsed in order to verify the time at which to charge the time cell again. Sakaki teaches all of the necessary structure, the methods of charging a charge storage element within controlling electrostatic discharge during and after discharging and charging states of a time cell in order to gain measurement of the elapsed time of the system and the corresponding charging and read operation steps needed to initialize and process the information of the apparatus are inherently possessed within said structure.

Regarding Claims 4-14, the combined teachings of Sakaki and Feddeler references inherently possess the methods of controlling electrostatic discharge during and after discharging and charging states of a time cell in order to gain measurement of the elapsed time of the system and the corresponding charging and read operation steps needed to initialize and process the information of the apparatus, as well as the ability to determine during the charging process the state of a time cell, specifically, whether the cells were successfully charged or not. It would be obvious to a person skilled in the art

at the time of the invention to recognize that because the Sakaki/Feddeler combination forms the structure of the inventive entity claimed, the methods needed to construct, charge/discharge, generate and read the components and data contained and produced are inherently possessed by the structure.

Regarding Claims 15-23, it would be obvious to a person skilled in the art at the time of the invention to construct a computer program to perform the method steps of Claims. It is well known in the art to build a computer program on a computer readable medium such as a floppy disk for easy insertion and data recall during use on a computer.

Regarding Claim 25, the Sakaki/Feddeler combination teaches the method comprising that a length of a predetermined time period varies with an initial threshold voltage of the floating gate field effect transistor after charging the floating gate (FIG. 1E-1J).

Regarding Claim 28, the combination of the Sakaki and Feddeler references teach a time cell, which has the ability of a conventional RC timer to measure electrostatic discharge in order to measure elapsed time. The Sakaki/Feddeler combination does not explicitly teach an article of manufacturing comprising a smart card. It would be obvious to a person skilled in the art at the time of the invention to adapt a smart card to include a charge storage device, e.g. an RC timer device in order to measure elapsed time of a charged storage element with a smart card in order to calculate the elapsed time memory has been stored on a smart card. Any capacitive timing device possesses

memory and means to store and read the memory and by applying this concept of measuring electrostatic discharge to calculate memory, a user may read the elapsed time a portion of memory that has been stored on the smart card and recharge or update the memory before it is erased.

Prior Art

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Ishibashi U.S. Patent No. 5,374,904 discloses a phase-locked loop circuit having adjustable reference clock signal frequency and filter capacitance compensation.
- Ma U.S. Patent No. 6,067,244 discloses a ferroelectric dynamic random access memory, wherein an FE transistor replaces a capacitor.
- Begin U.S. Patent No. 4,995,019 discloses a time period measuring apparatus wherein time measure is achieved by utilizing a time variable interpose, which comprises components that correspond to an RC circuit.
- Curtis U.S. Patent No. 5,195,061 discloses a practice timer for measuring elapsed time during an activity comprising a variable time constant RC circuit.
- Takeda U.S. Patent No. Re. 35,043 discloses a self-charging electronic timepiece comprising a time constant RC circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael L. Lindinger whose telephone number is (703) 305-0618. The examiner can normally be reached on Monday-Thursday (7:30-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Martin can be reached on (703) 308-3121. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7318 for regular communications and (703) 746-7318 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Michael L. Lindinger
Patent Examiner
Art Unit 2841

MLL
November 15, 2002

DAVID MARTIN
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